67A Hall Effect Joystick
I2C User Manual

Features
• Proportional digital output
• Shaft and panel seal to IP67
• Compact: 1-inch square flange
• Minimal 0.73-inch depth behind panel
• Long operational life > 1 million cycles

Applications
• Medical
• Material handling vehicles
• Mobile electronics for outdoor use

1 Introduction

The 67A joystick is a proportional output joystick which provides an X,Y coordinate (approx., 0-80) proportional to the joystick location. The X,Y coordinates are read from the joystick via an I^2C bus. Features include:

- Proportional Joystick
- I^2C Interface (other interfaces available)
- Low Operating Current (3 mA, max.@ V_{DD} = 3.3V)
- Low Power "Sleep Mode" (100 µA, max. @ V_{DD} = 3.3V)

2 Hardware Interface

2.1 Connector - Two options are available – header or ribbon cable with connector.

A. Ribbon cable with Tyco 7-215083-6 connector (Mating header: Tyco 7-215079-6).
B. Header (1x6) – 0.05" centers with 0.025" sq. pins.

Pin #	Signal	I/O	Description
1	SDA	I/O	I^2C Data Line
2	V_{DD}	-	Power Supply. 3.0V – 3.6VDC
3	V_{SS}	-	Ground
4	SCL	In	I^2C Clock Line
5	INTn	Out	Interrupt Out. Open Drain. Active Low.
6	A1n	In	A1n (LSB) of 7 bit I^2C address

Table 1: 67A Connector Signals

The 67A is an I²C (Slave) with 7 bit I²C address of 80h (A1n floating) or 82h (A1n tied to Gnd).
I²C speed: up to 400 KHz.
External pull-up resistors are required for I²C signals (SDA & SCL- See Sec 2.3 for recommended pull-up resistors for I²C signals) and INTn (Recommended value 2K-10K).
(See Fig. 1)

INTn – Interrupt Out (Active Low) - Goes low only when a different X, Y value is available. Reading the Y value causes INTn to go high (inactive). For most efficient use of the I²C bus and processor resources it is recommended that the INTn signal be used to trigger reading of the X, Y value from the joystick. If INTn is not used, X, Y values should be read continuously at a rate of 50 samples/sec. An external pull-up resistor in the range of 2K - 10K (see Fig. 1) is required for INTn.

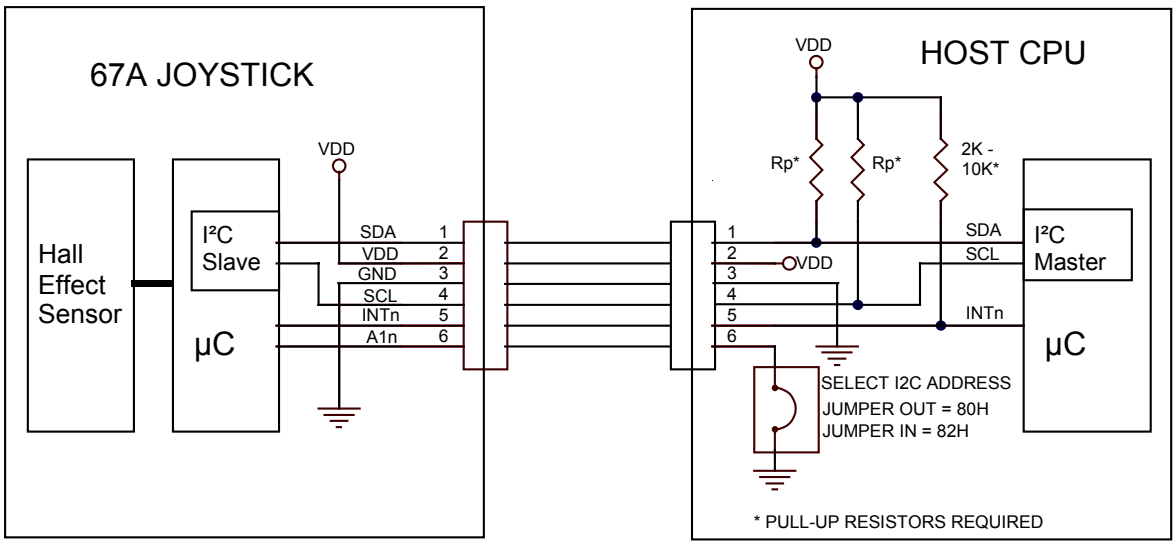

FIG 1 – 67A Electrical Connection Diagram

2.2 Cable/PCB Trace Length

Cable/PCB Trace Length: Varies with I²C frequency. The I²C Spec. specifies a max. capacitance per signal line (SCL or SDA) of 400 pF. The bus capacitance is the total of wire, PCB traces and pins. The longer the cable/PCB trace length the higher the bus capacitance and thus, the lower the operating frequency that can be used.

2.3 Pull-up Resistors

2.3.1 I²C Signals (SCL, SDA) Pull-up Resistors

The two I²C signals (SDA & SCL) must be pulled up to the power supply voltage at the Host CPU. The pull-up resistor value depend on the bus capacitance and SCL frequency. See Table 2 below for recommended pull-up resistor values vs. SCL frequency and bus capacitance:

	Rp recommended			
	Bus Load Capacitance			
SCL Frequency	100 pF	200 pF	300 pF	400 pF
Standard Mode (100 KHz)	6.49KΩ	3.48KΩ	2.49KΩ	2KΩ
Fast Mode (400 KHz)	2.26KΩ	1.4KΩ	1.1KΩ	

Table 2 - Recommended Pull-up Resistors for SCL, SDA vs. Frequency & Bus Capacitance

To determine if a proper pull-up value is being check the low and high voltage levels for SCL and SDA during I²C bus activity. The signal levels should meet the following requirements with at least a 0.1V margin:

$$V_{L,\,MAX} < 0.3\ V_{DD}$$
$$V_{H,\,MIN} > 0.7\ V_{DD}$$

For more on choosing the I²C pull-up resistors see: Sec. 7.1 in *I2C-bus specification and user manual, Rev. 03* (NXP UM10204).

2.3.2 INTn Pull-up Resistor

The pull-up for the INTn signal should be between 2K-10KΩ.

3 I²C Interface

The 67A joystick communicates over an I²C bus (2-wire bi-directional serial interface). The host CPU (master) must initiate the data transfers, as the 67A is a slave device.

I²C address - The I²C address consists of 7 bits (D7-D1) and a bit (D0) indicating whether it is a Read (1) or Write (0) cycle. The 67A is shipped from the factory with the 7-bit device I²C address of 80H ('1000 000X') when A1n (pin 6) is left floating (not connected). The I²C address may be changed to 82H by pulling A1n to Gnd. If A1n is changed after power-up then a reset command needs to be sent to the joystick to make active the new value (A1n is only read by the joystick after a power-up or reset command). Changing the I²C address would be necessary if two 67A joysticks are connected to the same I²C bus or if another component connected to the I²C bus shared the same I²C address. To request a custom I²C address contact Grayhill.

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SDA is a bi-directional signal and is used to read and write the serial data. The SCL signal is the clock generated by the host CPU, to synchronize the SDA data in read and write mode. The maximum I²C clock frequency is 400 KHz with data triggered on the rising edge of SCL.

Clock Stretching - Clock stretching occurs when a device on the bus holds the SCL line low effectively pausing communication. The joystick (slave) may stretch the clock to allow more time to load data to be read by the master device. It is important that the I²C Master interfacing with the 67A implement clock stretching on a byte level for reliable operation with the joystick. See Sec. 5.1.1 for more on clock stretching.

3.1 I²C Registers

3.1.1 X Register

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
X(7) sign	X(6) MSB	X(5)	X(4)	X(3)	X(2)	X(1)	X(0) LSB
R	*R*	*R*	*R*	*R*	*R*	*R*	*R*

Reset value: 0000 0000
• Bit7-0: X coordinate

X coordinate, 2's complement format (signed –128 to +127).
Note: After every complete I^2C transaction the register pointer in the joystick is set to point at the X register so that X register value can be read without writing to register pointer (See Sec. 3.2).
IMPORTANT: In order to keep X & Y values paired together or "in synch.", X register data should be read in an I2C sequence which reads both the X & Y registers as described in Sec. 3.2.1. and Fig. 2.

3.1.2 Y Register

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Y(7) sign	Y(6) MSB	Y(5)	Y(4)	Y(3)	Y(2)	Y(1)	Y(0) LSB
R	*R*	*R*	*R*	*R*	*R*	*R*	*R*

Reset value: 0000 0000
• Bit7-0: Y coordinate

Y coordinate, 2's complement format (signed –128 to +127)
Reading the Y register will reset INTn output to Hi-Z.
The Y register should be read in a single I2C sequence that reads the X Register first immediately followed by the Y register as described in Sec. 3.2.1. and Fig. 2.

3.1.3 Control Reg. (76h)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
X	X	X	X	X	X	Reset	X
						W	

X = Do Not Care
Reset value: 1001 1010 (9Ah)

Writing to this register with Reset (Bit 1) high resets joystick and sets all registers to default values. The Reset bit is set low by the joystick after completing the reset sequence. Note: there is a start-up time ($T_{P,W}$) which must be observed after resetting the joystick.

3.2 I^2C Read and Write Cycles

3.2.1 Read X & Y Values – When INTn goes low there are new X & Y values available. To read the X & Y values the external I^2C Master should perform a read sequence of 2 bytes <u>without</u> providing a register address (Joystick always sends X register value followed by Y register value for any 2 byte read without a register address). INTn will go high (inactive) at the beginning of the read of the Y value (see Fig. 2).

I^2C Start Command
81h or 83h (Joystick I^2C Address with D0 set for read)
X Byte (Data from Joystick)
Y Byte (Data from Joystick)
I^2C Stop Command

<u>Important Note</u>: If a new X & Y value is available before the previous values are read the new values will over-write the old (with the loss of the oldest values). However, in order to keep the X & Y values paired together or "in sync", <u>it is important that the user read the X & Y values in the a single I^2C sequence as shown in Fig. 2</u>. This is also the fastest and most efficient use of the I^2C bus.

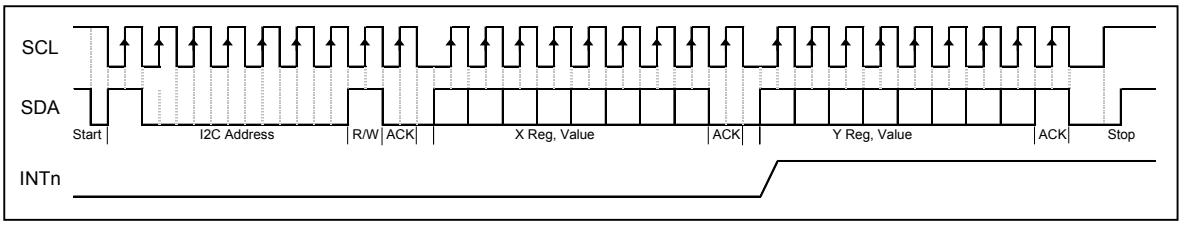


FIG. 2 – Read X & Y Values over I²C Bus

3.2.2 Reset Joystick – To reset the joystick the I²C Master should perform a write sequence of 1 byte and must provide the register address for Control Reg. :

I²C Start Command
80h or 82h (Joystick I²C Address with D0 low for write)
76h (Register Address for Control Reg.)
9Ah (Data)
I²C Stop Command

Note: after sending the reset command the I²C Master must wait 300 ms before attempting to access the 67A. At the end of the Nominal Startup Time ($T_{P,W}$) the 67A generates the first XY pair of values and sets INTn low. Thereafter INTn goes low only if the X or Y value changes.

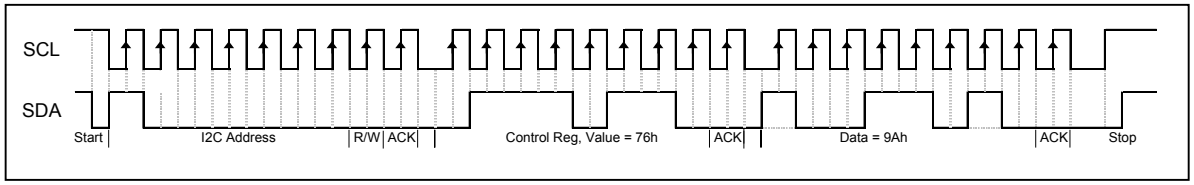
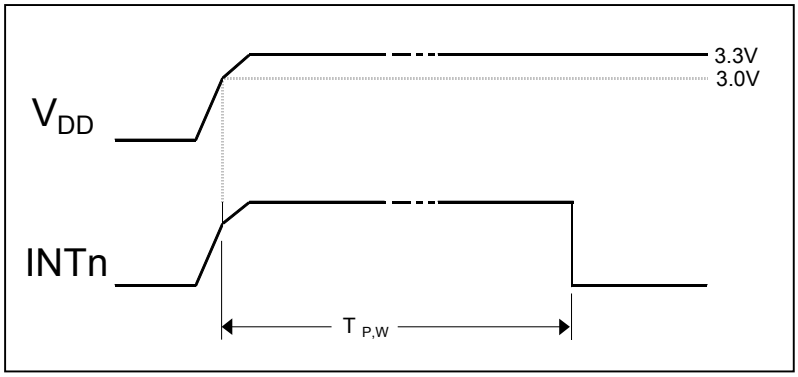


FIG. 3 – Send Reset Command over I²C Bus

4 Power Modes & Sleep Threshold

4.1 **Power Up Sequence** – During a power-up once the power supply voltage reaches 3.0V the user must wait the Nominal Startup Time ($T_{P,W}$) before communicating with the joystick over the I²C bus (also applies to a reset joystick command). At the end of the Nominal Wakeup Time the 67A generates the first pair of XY values and sets INTn low. Thereafter INTn goes low only if the X or Y value changes

FIG. 4 – Power Up Sequence



4.2 **Full Power Mode:** In this mode an internal measurement occurs every 20 ms. If the X or Y value changes from the last values ouptut, the INTn output (Pin 5) is set low signaling new X & Y values are ready to be read. INTn is cleared (Hi-Z) while the Y value is read. Power consumption is higher in this mode. As long as the joystick position is outside of the Sleep Zone, it will operate in this mode.

4.3 Low Power (Sleep) Mode: When the joystick position for both X and Y is within a circle defined as the Sleep Zone for ten consecutive measurements the joystick goes to the Low Power mode where power is significantly lower. The Sleep Zone typically extends to a joystick shaft angle of 5° from the center (See Fig. 6). The last XY value output before entering the Low Power mode is (0,0). As long as the joystick remains within the circle defined by the threshold, the joystick will remain in the Low Power Mode and INTn will stay high. When the joystick is moved outside of the Sleep Zone circle, it returns to the Full Power mode, new XY measurements are available every 20 ms and power consumption increases. Low Power (Sleep Mode) current may be higher if supply voltage drops below 2.9V.

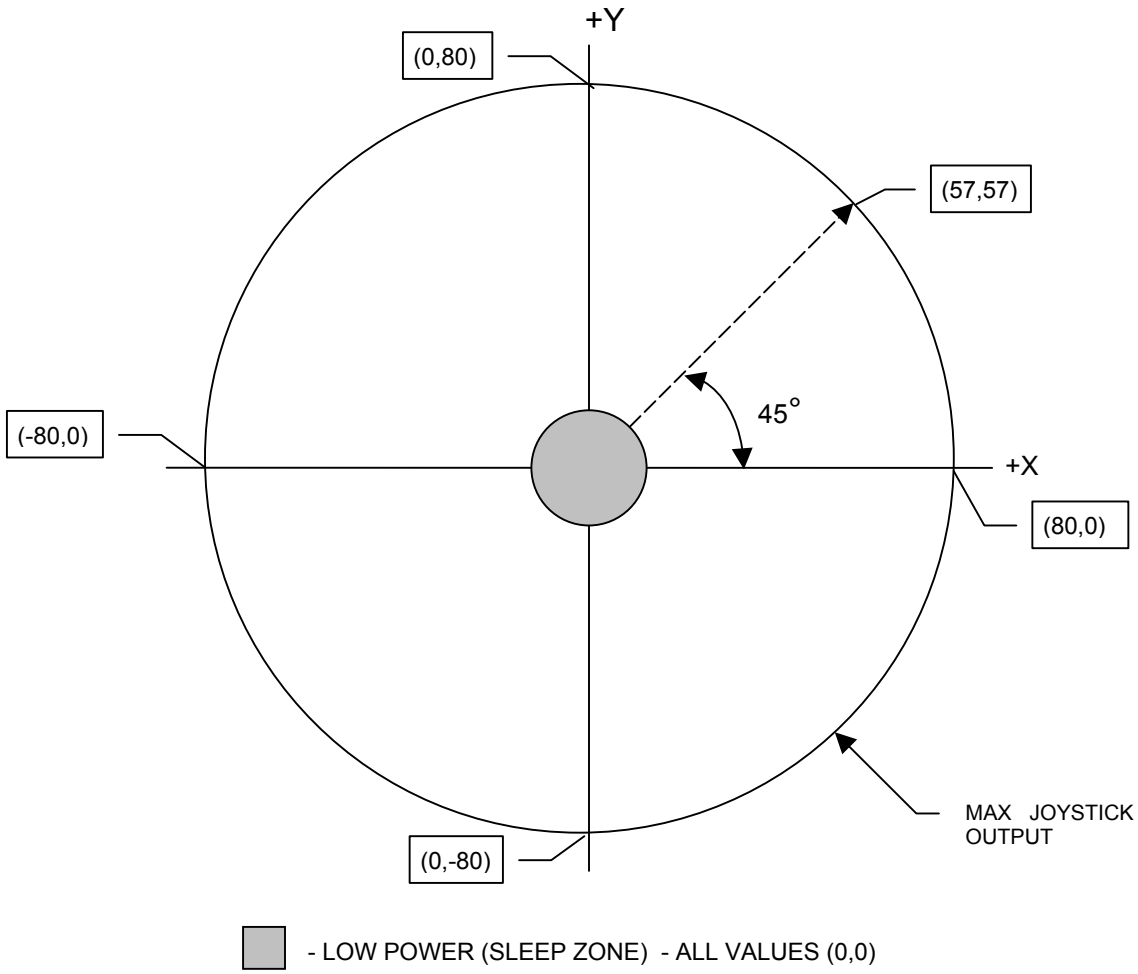


FIG. 5 – Sleep Zone & Max. Output Circle

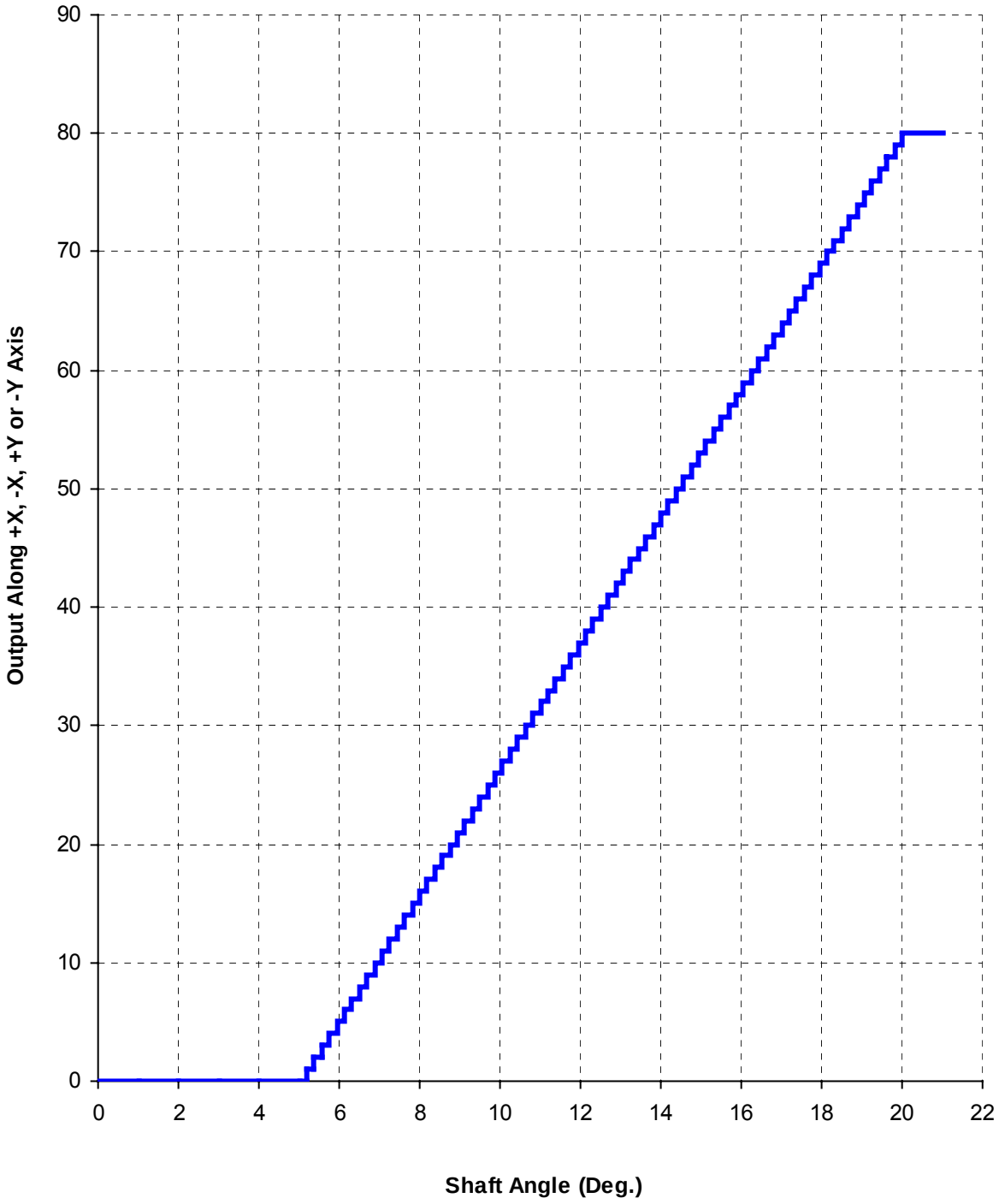


FIG. 6 – Joystick Output Along X or Y Axis vs. Shaft Angle (Typical)

5 SPECIFICATIONS

NOTICE: Stresses above those listed under "Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device above those listed in the operation listings of this specification is not implied. Exposure above maximum ratings conditions for extended periods may affect device reliability.

Table 3 - Absolute Maximum Ratings (non operating)

Parameter	Sym.	Min	Max	Unit	Note
DC Supply Voltage	V_{DD}	-0.3	4.0	V	
Voltage on all other pins with respect to Vss	V_{IN}	-0.3	V_{DD} + 0.3	V	
Max current sunk by any I/O pin			25	mA	
Storage temperature	T_{strg}	-55	+100	°C	

Table 4 - Operating Conditions

Parameter	Sym.	Min	Typ	Max	Unit	Note
DC Supply Voltage	V_{DD}	3.0	3.3	3.6	V	
High level input voltage	V_{IH}	0.7 V_{DD}			V	SCL, SDA
		0.25 V_{DD} + 0.8			V	A1n
Low level input voltage	V_{IL}			0.3 V_{DD}	V	SCL, SDA
				0.15 V_{DD}	V	A1n
Leakage Current	I_{IL}	-	±5	±125	nA	$V_{SS} \le V_{PIN} \le V_{DD,}$ Pin at high impedance at 85°C
Low level output voltage	V_{OL}			0.6	V	INTn , SDA I_{OL} = 6mA, V_{DD} = 3.3V
Current Consumption, Full Power mode (V_{DD} = 3.3V)	I_{DD1}		2.5	3.0	mA	Average current V_{DD} pin
Current Consumption, Low Power (sleep) mode (V_{DD} = 3.3V)	I_{DD2}		50	100	µA	Average current V_{DD} pin. Note 3.
Measurement Frequency, (Full Power mode)			50		Sample s/sec	
Response Time (Full Power Mode)				20	ms	Note 2
Response Time (Low Power Mode)				80	ms	Note 2
Output with Max. Joystick Deflection	X_{MAX} or Y_{MAX}	±79	±80	±80	Units	Notes 1, 4
Output with Joystick Released (Center)	$X_{MIN,}$ or Y_{MIN}	-	0	0	Units	
Low Power (Sleep) Threshold			5		Deg	
Nominal Startup Time	$T_{P,W}$			300	ms	
Operating temperature range	T_{amb}	-40		+85	°C	

Note 1: Positive value is for movement in the positive X or Y direction. Negative value is for movement in the negative X or Y direction. Positive Y direction is indicated by the ▲ symbol on the joystick case.

Note 2: Response time is the time from joystick movement to when new X,Y position data is available (INTn goes low).

Note 3: For VDD <2.9V current will exceed 100 uA .

Note 4: Max. values along X or Y axis in positive and negative directions.

5.1 I²C Bus Timing Requirements

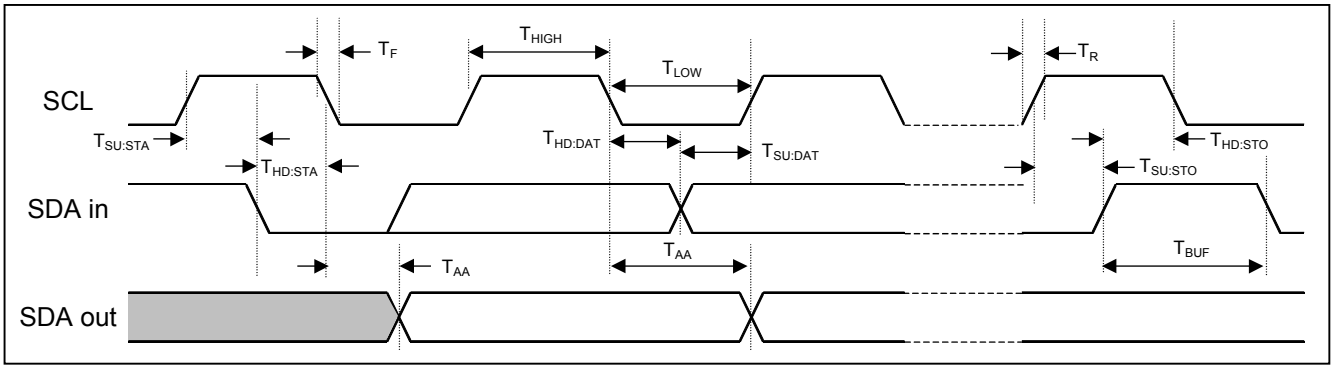


FIG. 7 - I²C Bus Data Requirements

Table 5 - I²C Bus Data Requirements

Parameter		Sym.	Min	Typ	Max	Unit	Note
Start condition Hold time	100 kHz mode	T HD:STA	4000	—	—	ns	After this period, the first clock pulse is generated
	400 kHz mode		600	—	—		
Stop condition Setup time	100 kHz mode	T SU:STO	4700	—	—	ns	
	400 kHz mode		600	—	—		
Stop condition Hold time	100 kHz mode	T HD:STO	4000	—	—	ns	
	400 kHz mode		600	—	—		
Clock high time	100 kHz mode	T HIGH	4.0	—	—	µs	
	400 kHz mode		0.6	—	—		
Clock low time	100 kHz mode	T HIGH	4.7	—	—	µs	
	400 kHz mode		1.3	—	—		
SDA and SCL rise time	100 kHz mode	T R	—	—	1000	ns	
	400 kHz mode		20 + 0.1CB	—	300		CB is specified to be from 10-400 pF
SDA and SCL fall time	100 kHz mode	T F	—	—	250	ns	
	400 kHz mode		20 + 0.1CB	—	250		CB is specified to be from 10-400 pF
Data input hold time	100 kHz mode	T HD:DAT	0	—	—	ns	
	400 kHz mode		0	—	0.9	µs	
Data input setup time	100 kHz mode	T SU:DAT	250	—	—	ns	(Note 2)
	400 kHz mode		100	—	—	ns	
Output valid from clock	100 kHz mode	T AA	—	—	3.5	µs	(Note 1)
	400 kHz mode		—	—	—	ns	
Bus free time	100 kHz mode	T BUF	4.7	—	—	µs	Time the bus must be free before a new transmission can start
	400 kHz mode		1.3	—	—		
SCL delay from Clock Stretching	Full Power Mode	T DEL	—	20	—	µs	See Fig. 8
	Low Power Mode		—	45	—		
Bus capacitive loading		CB	—	—	400	pF	

Note 1: As a transmitter, the device must provide this internal minimum delay time to bridge the undefined region (min. 300 ns) of the falling edge of SCL to avoid unintended generation of Start or Stop conditions.

Note 2: A Fast mode (400 kHz) I^2C bus device can be used in a Standard mode (100 kHz) I^2C bus system, but the requirement $T_{SU:DAT} \geq 250$ ns must then be met. This will automatically be the case if the device does not stretch the low period of the SCL signal. If such a device does stretch the low period of the SCL signal, it must output the next data bit to the SDA line T_R max. + $T_{SU:DAT}$ = 1000 + 250 = 1250 ns (according to the Standard mode I^2C bus specification), before the SCL line is released.

5.1.1 Clock Stretching

As mentioned previously the I2C Master that interfaces with the joystick must be capable of clock stretching on a byte level. The joystick is able to transmit a byte of data at a fast rate, but may need more time to prepare the next byte to be transmitted. The joystick (slave) holds the SCL line LOW after transmission and acknowledgment of a byte to force the master into a wait state until the slave is ready for the next byte transfer in a type of handshake procedure (See Fig. 8 below). See I^2C Spec. UM10204, Rev. 3, Sec. 3.9 for more on clock stretching.

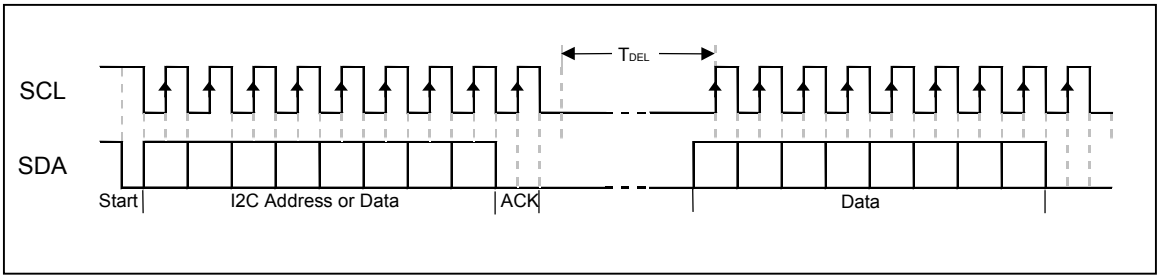


FIG. 8 – Clock Stretching by Joystick

Revision History

Date	Rev	Name	Description of Changes
07/25/12	1.0	SAK	Initial Version – Started from V2.3 of Electrical Spec.
9/18/12	1.1	SAK	Replaced Fig. 6 (Joystick Output vs. Shaft Angle) with more accurate graph and changed graph labels.
9/19/12	1.2	SAK	Corrected Fig. 5 graphic